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Title:	6U SpaceVPX/OpenVPX Payload Processor
Author(s):	Graham, Paul Stanley Merl, Robert Bernard Nelson, Anthony Edward
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6U SpaceVPX/OpenVPX Payload Processor

Robert Merl, ISR-4
Anthony Nelson, ISR-4
Paul S. Graham, ISR-3

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Space-Grade Single-Board Computer

- 6U Eurocard VPX
  - 230 mm x 160 mm
  - Interoperable between OpenVPX and SpaceVPX
  - Complies with ANSI/VITA 65 and 78
    - SLT6-SWH-16U20F-10.4.2 and SLT6-SWC-12F16T-10.4.1 System Controller and Switch slot profiles
- For use in GEO / MEO / LEO Orbits
  - 100-krad TID
  - Latch-up immunity: 103 MeV/mg/cm^2
  - Mechanically Hardened
  - Meets or exceeds NASA GEVS for shock, vibration, thermal
  - Conduction-cooled Frame
  - Hypertac Connectors
  - QML-V or Class S components
- Low Power / 8.5 W

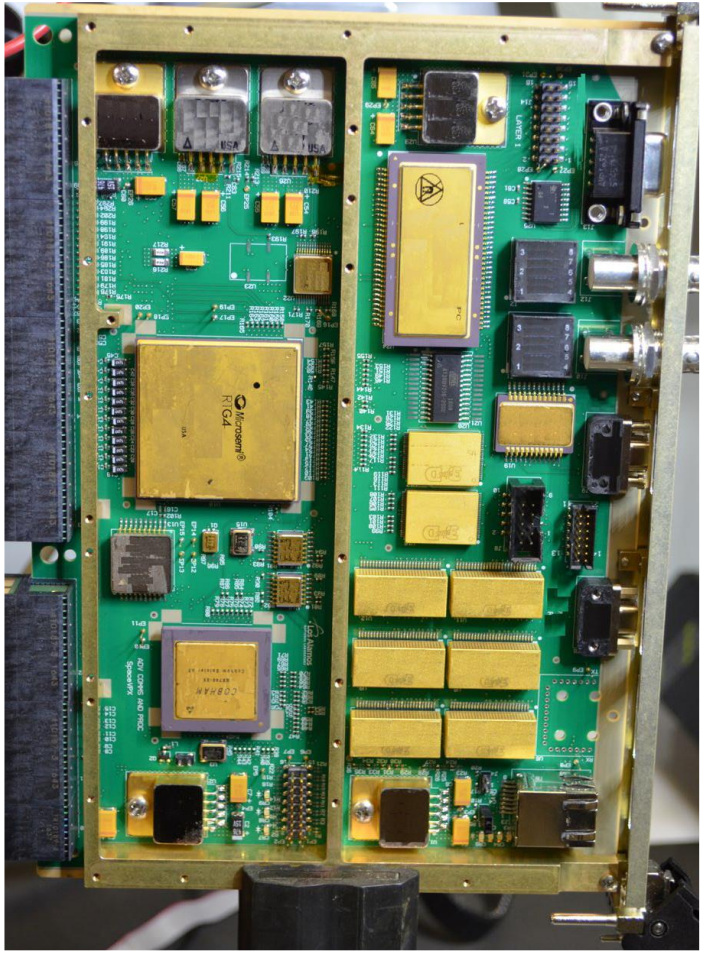
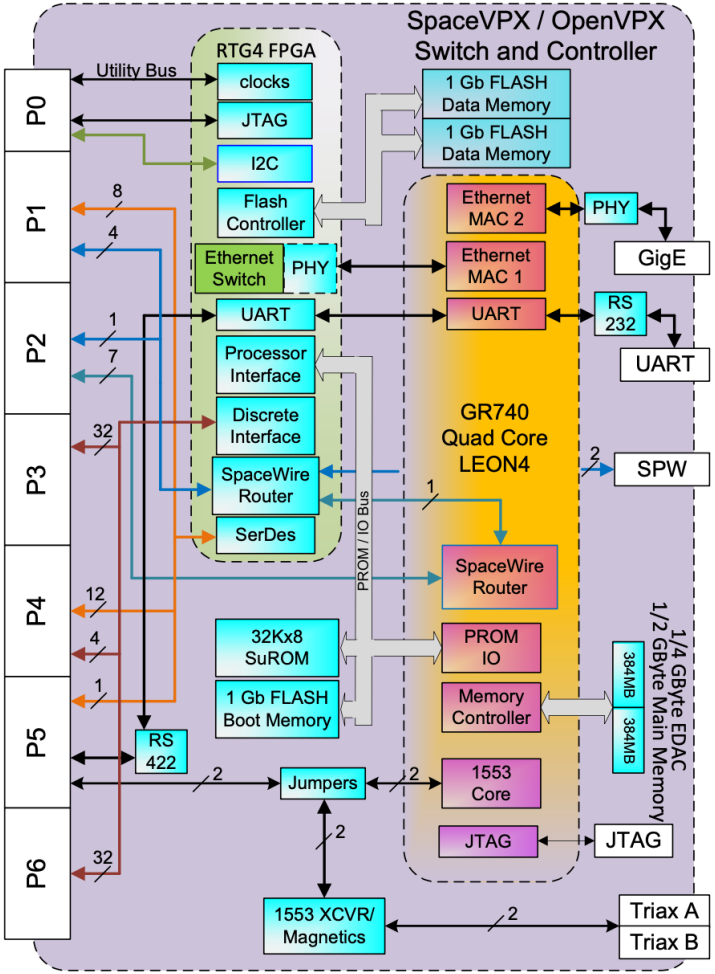


Image of first revision of the 6U OpenVPX/SpaceVPX processor board

Flexible and Reconfigurable

- CAES Quad-Core LEON4 GR740 Processor
  - GFLOP performance
  - 512 Mbyte of SDRAM / 256 Mbyte of EDAC
  - 384 Mbyte of Non-Volatile Storage
  - PROM / Flash / SDRAM memory hierarchy
- VxWorks RT Operating System
- Reconfigurable Microchip RTG4 FPGA
- Common Space-Grade Interfaces
  - SpaceWire
  - I2C
  - Discrete I/O (single-ended and differential)
  - MIL-STD-1553B (can drive front-panel connectors ***or*** drive XCVR and magnetics on a separate interface board)
  - RS-422 UART
  - Multi-gigabit serial transceivers
    - The Ethernet PHY in the RTG4 is under development—initial use is for a possible point-to-point connection over the backplane.
    - The Ethernet Switch in the RTG4 is a ***future*** option not implemented in the current firmware.

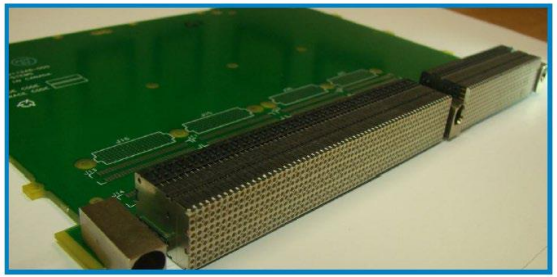


Block diagram of the 6U OpenVPX/SpaceVPX processor card

Commercial Interoperability

- Interoperates with commercial backplanes, enclosures, modules, and test equipment
- Can be inserted into flight-like systems late in the design cycle
- Designed for assembly with low-cost commercial VPX connectors or flight-grade Hypertac connectors in the same footprints

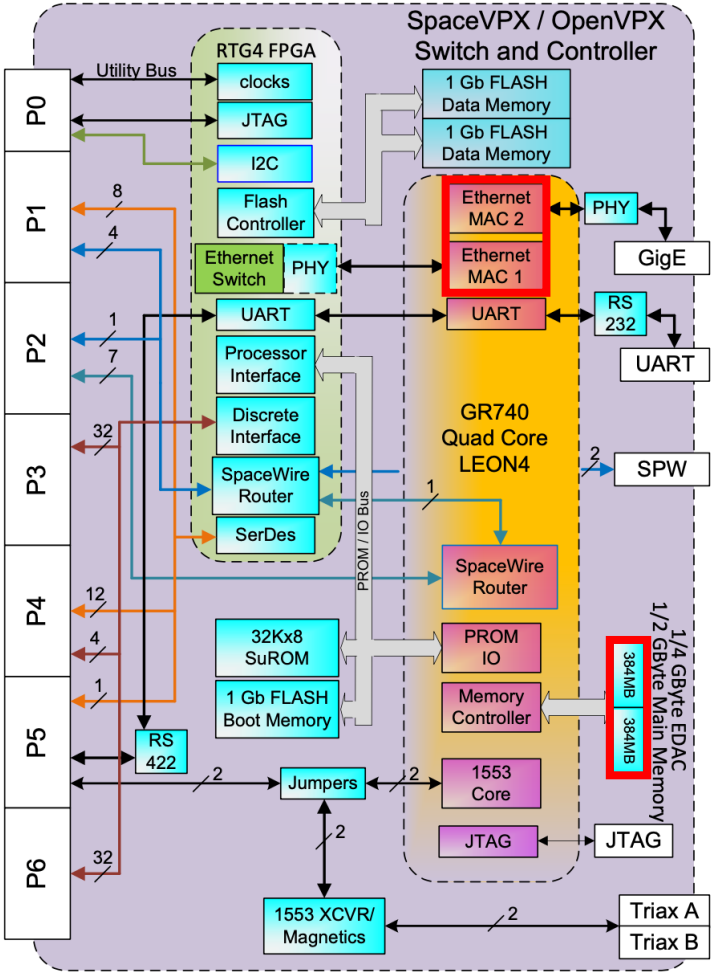
Los Alamos designed SpaceVPX System Controller in commercial system



Design Trade-Offs: SDRAM Density vs. Ethernet Connectivity

- In improving the memory performance from the first revision of the board, we encountered the following trade-off:
  1. Include 1 GiB of EDAC-protected SDRAM (1 GiB of usable memory with 0.5 GiB of EDAC), but have only one Ethernet connection from the GR740
     - To provide 1 GiB of SDRAM, we must use a 96-bit-wide SDRAM memory interface on the GR740 due to the architecture of the SDRAM modules that were used. Early simulations suggest that the RAM can run at 50 MHz, which is effectively the same bandwidth as a 48-bit-wide SDRAM interface running at 100 MHz.
     - Unfortunately, the 96-bit-wide SDRAM interface conflicts with one of the two Ethernet ports from the GR740. The Ethernet port to the RTG4 would be the port that we would drop since the one on the front panel would be easier to use for flight software development. The front-panel Ethernet could be used for flight with the appropriate connector.
  2. Include only 0.5 GiB of EDAC-protected SDRAM (0.5 GiB of usable memory with 0.25 GiB of EDAC), but have both Ethernet connections from the GR740
     - Using the same SDRAM modules, going to a 48-bit-wide SDRAM interface reduces the usable SDRAM by 50% due to limitations on the chip selects available from the GR740. Early simulations suggest that the SDRAM will run at 70-80 MHz, possibly faster. This option provides more clock margin for the SDRAM.
     - Both Ethernet ports are available, one to the front panel for development and another to the RTG4 for ***future support*** of SERDES-based Ethernet (1000BASE-KX/BX)
       - A point-to-point SERDES Ethernet connection to another VPX module (demonstration in development)
       - An Ethernet switch in the RTG4 available to multiple modules via SERDES (possible future development)

Given our internal SDRAM needs, we chose Option 2 to provide future connectivity options and more clock margin for the SDRAM.



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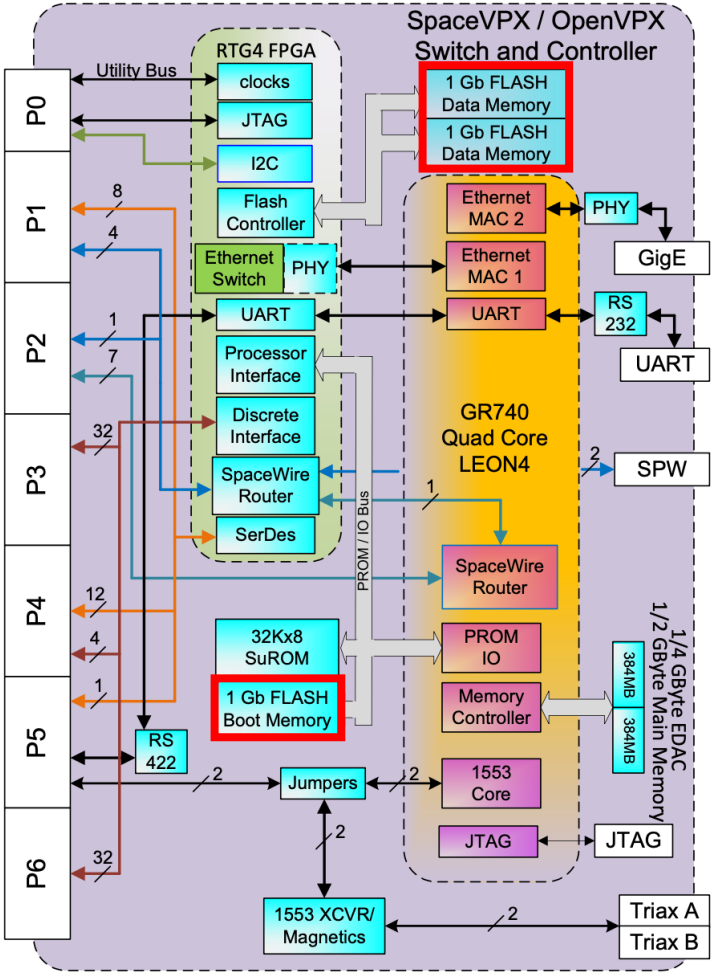
Design Trade-Offs: Non-volatile Storage Density vs. Hardness

- The original design had 2 GiB of NAND flash, but those memories were limited to 70-krad TID even after extra screening.
- Internal customers prioritized radiation hardness over storage density for the non-volatile memory, so we chose to use CAES 128-MiB, 300-krad TID NOR flash for this design, for a total of 384 MiB of storage.
  - 256 MiB of data storage (behind the RTG4 due to limited chip selects on the PROM/IO bus)
  - 128 MiB of boot storage (replacing an 8-MiB MRAM)



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